VRAM Interface
Functional Specification

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Contents:

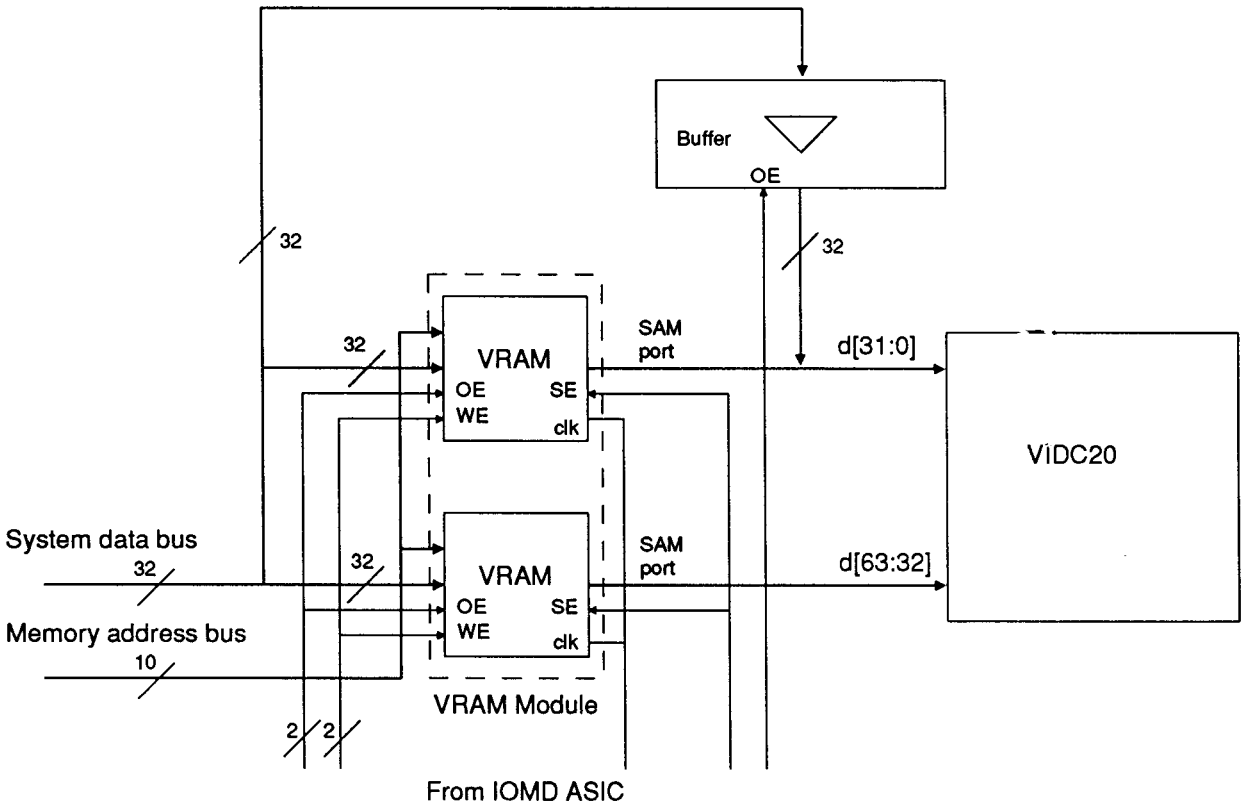
1. Introduction

The product is the first Acorn platform to allow Video RAM (VRAM) to be fitted. The system controller IC; IOMD uses the video controller IC; VIDC20 in it's 64 or 32 bit wide DRAM modes but interfaces it with VRAM instead. This allows the video system to operate at any speed whilst not affecting the overall system memory bandwidth. VRAM is dual ported so that screen updating is automatically handled by VIDC20 reading from the second port of the dual ported VRAM, whilst any access to Video memory from the main system occurs as though it was normal memory. The access does not affect and is not affected by the screen being updated from the second port by the video controller IC (VIDC20).

A 136 way dual read-out SIMM (DIMM) connector is provided which allows a module to be fitted holding either 1 or 2MB of VRAM. This is arranged as one or two 1MB banks of 256K x 32 bits each. A suitable VRAM IC would have a DRAM port of 256k x 8 bits, and a split transfer Serial Access Memory (SAM) port of 512 x 8 bits. Eight of these are needed for a 2MB VRAM module. Bulk and high frequency decoupling components must also be fitted to the module PCB.

Although the platform has been designed to accommodate only 1 or 2 MB modules there may be a requirement for a larger module at a later stage of production, and support for this is provided by the addition of address line Ra<9>. The design of IOMD is such that it can address up to 16 MB of VRAM, but because address lines Ra <9:0> only are tracked to the VRAM module connector a total of 8MB of address space is available for VRAM. However, use of larger VRAM modules will require suitable address mapping logic.

1. 1 System Diagram



2. System Operation

If unfamiliar with Video RAM operation, the reader is referred to a suitable VRAM data sheet for an explanation of the terms used here.

The video interface is designed to support VIDC20 used with either DRAM or VRAM. The VIDC20 VRAM interface mode is not used, instead, VIDC20 is used either in 32 bit DRAM interface mode for DRAM or one bank of VRAM, or in 64-bit DRAM interface mode with two banks of VRAM. Cursor, sound and programming information comes from the main data bus, as does the video data when the VRAM is not used. When used, the VRAM SAM ports connect directly to the VIDC20 data input ports, The system data bus is normally isolated from the data port by a '244 type buffer. An active low output enable signal (Ncdoe) is generated by IOMD to control the buffer. The serial port of the VRAM connected to d[31:0] of VIDC must be disabled during cursor DMA (horizontal retrace time), programming and sound DMA. When both banks of VRAM are fitted, the Nwe and Noe/dt lines are used to interleave the VRAM banks on the memory bus side on a word basis, using A[2] to select the bank required.

At the start of each frame, IOMD does a full transfer to the VRAM, to initialise the video pointer in the SAM. It then does split transfers whenever needed, as indicated by the qsf pin of the VRAM. The full-transfer is done on the last but one line of the flyback period. This is to ensure that the VRAM SAM port is loaded with new data if the frame buffer has been updated during flyback.

For detailed timing and operational information, the reader is referred to the IOMD and VIDC20 datasheets.

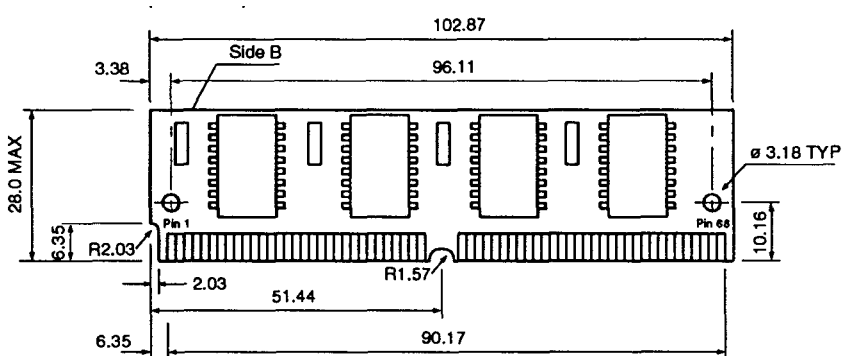
3. VRAM Module Physical Description

The VRAM Module is a double sided PCB designed to hold either one or two MBytes of Video RAM. The PCB is inserted into the dual read-out SIMM socket (DIMM socket) on the motherboard. The operating system recognises when the module is present and takes advantage of the extra memory bandwidth provided automatically by changing over from main DRAM.

The following specifications define the physical construction of a suitable VRAM card, along with the electrical requirements which the component VRAM ICs must meet.

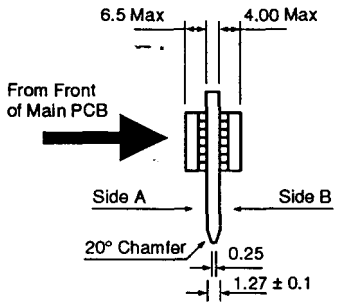
3.1 Physical Dimensions and Pin Orientation

Front View (Side A)

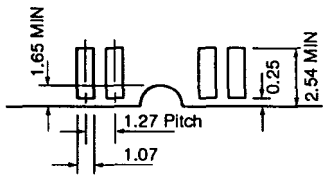


Side A Pin 1 & Side B Pin 1 are adjacent

Side View



Contact Detail



Contacts to be Gold Plated
& Centered on PCB edge

All dimensions in mm
Tolerances: ± 0.2 unless specified

The number & orientation of ICs on this module is for guidance only

3.2.1 Signal List

VRAM Signal	Description
Ud[31:0]	Upper Bank 32 bit SAM port data bus (VIDC Din<63..32>)
Vcd[31:0]	Lower Bank 32 bit SAM port data bus (VIDC Din<31..0>)
Rd[31:0]	32 bit DRAM port data bus
Ra[9:0]	10 bit DRAM port address bus
Cas[3:0]*	4 CAS lines (select byte within word for both banks)
VRas*	RAS line for all VRAM ICs
We[1:0]*	Write Enable, one for each bank
Dt[1:0]*	Data Transfer (Output Enable), one for each bank
Sc	Serial Port control clock
Se*	Serial Port Enable
Dsf	Special Function input
Qsf	Special Function output
Vdd	5 Volt supply ('5 Pins)
0v	Zero Volt, Digital ground (12 Pins)

3.2.2 Connector Pinout

Pin No	Side A	Side B	Pin No	Side A	Side B
1	Ud<0>	0V	35	Vcd<8>	+5V
2	0V	Vcd<7>	36	Ud<13>	Sc
3	Ud<1>	Vcd<6>	37	Vcd<9>	Se*
4	Ud<2>	Vcd<5>	38	Ud<12>	Qsf
5	Ud<3>	+5V	39	Vcd<10>	Dsf
6	Ud<7>	Vcd<4>	40	Vcd<11>	Cas<0>*
7	Vcd<0>	Rd<0>	41	+5V	Cas<2>*
8	Ud<6>	Rd<16>	42	Vcd<15>	Cas<3>*
9	Vcd<1>	Rd<1>	43	Ud<8>	Cas<1>*
10	+5V	Rd<17>	44	Vcd<14>	Vras*
11	Ud<5>	Rd<2>	45	Ud<9>	Dt<0>*
12	Vcd<2>	Rd<18>	46	Vcd<13>	Dt<1>*
13	Ud<4>	Rd<3>	47	Ud<10>	We<0>*
14	Vcd<3>	Rd<19>	48	0V	We<1>*
15	Vcd<23>	0V	49	Vcd<12>	0V
16	Ud<16>	Rd<22>	50	Ud<11>	Rd<8>
17	Vcd<22>	Ra<0>	51	Vcd<24>	Rd<24>
18	Ud<17>	Ra<1>	52	Vcd<25>	Rd<9>
19	Vcd<21>	Ra<2>	53	Vcd<26>	Rd<25>
20	0V	Ra<3>	54	0V	Rd<10>
21	Ud<18>	Ra<4>	55	Vcd<27>	Rd<26>
22	Vcd<20>	Ra<5>	56	Ud<31>	Rd<11>
23	Ud<19>	Ra<6>	57	Ud<30>	Rd<27>
24	Ud<23>	Ra<9>	58	Ud<29>	Rd<12>
25	Ud<22>	Rd<4>	59	Ud<28>	0V
26	Vcd<16>	Rd<20>	60	+5V	Rd<28>
27	Ud<21>	Rd<5>	61	Vcd<31>	Vcd<30>
28	Vcd<17>	Rd<21>	62	Vcd<29>	Rd<29>
29	Ud<20>	0V	63	Vcd<28>	Rd<13>
30	Vcd<18>	Rd<6>	64	Ud<24>	Rd<30>
31	Vcd<19>	Rd<7>	65	Ud<25>	Rd<14>
32	0V	Rd<23>	66	Ud<26>	Rd<31>
33	Ud<15>	Ra<7>	67	Ud<27>	Rd<15>
34	Ud<14>	Ra<8>	68	0V	0V

4.1 AC Characteristics (Correspondent with VRAM IC data sheet)

PARAMETER	SYMBOL	MIN/MAX	VALUE	UNITS
Random Read or Write Cycle	(tRC)	min	150	ns
Page Mode Read or Write Cycle	(tPC)	min	55	ns
RAS Precharge Time	(tRP)	min	55	ns
Row Address Set-up Time	(tASR)	min	0	ns
Row Address Hold Time	(tRAH)	min	12	ns
Column Address Set-up Time	(tASC)	min	0	ns
Column Address Hold Time	(tCAH)	min	20	ns
Access Time from RAS	(tRAC)	max	70	ns
Access Time from CAS	(tCAC)	max	20	ns
Access Time from CAS Precharge	(tCPA)	max	45	ns
Column Address Access Time	(tAA)	max	40	ns
RAS Pulse Width	(tRAS)	min	70	ns
CAS Precharge Time(FP Mode)	(tCP)	min	20	ns
CAS to RAS Precharge Time	(tCRP)	min	20	ns
Write Command Set-up Time	(tWCS)	min	0	ns
Write Command Hold Time	(tWCH)	min	15	ns
Read Command Set-up Time	(tRCS)	min	0	ns
Read Command Hold Time	(tRCH)	min	0	ns
Write Command Pulse Width	(tWP)	min	15	ns
Data in Setup Time	(tDS)	min	0	ns
Data in Hold Time	(tDH)	min	20	ns
CAS Setup Time, CBR Refresh	(tCSR)	min	10	ns
CAS Hold Time, CBR Refresh	(tCHR)	min	20	ns
OE Access Time	(tOE)	max	25	ns
SAM port cycle time	(tSCC)	min	40	ns
Access time from SC	(tSCA)	max	25	ns
SC Precharge Time, SC Low	(tSP)	min	10	ns
Access time from SE*	(tSEA)	max	25	ns
Serial data-out hold time after SC hi	(tSOH)	min	5	ns
SC Low Hold Time after Dr	(tSDH)	min	25	ns
Split Transfer Setup Time	(tSTS)	min	70	ns
DT* to RAS* Setup Time	(tDTS)	min	0	ns
DT* to RAS* Hold Time (DT* HI)	(tDTH)	min	15	ns
DT* to RAS* Hold Time (DT* LO)	(tRDHS)	min	25	ns
DSF* to RAS* Hold Time	(tRFH)	min	15	ns
Output Disable Time From SE*	(tSEZ)	max	20	ns
Refresh Period for 512 cycles	(tREF)	max	8	ms

The above figures are given for correspondence with a typical VRAM data sheet. For example, a suitable part must operate with a minimum value of tRC no greater than 150 ns, or a maximum value of tREF which is no greater than 8 ms.

4.2 Capacitive Loading (2 MB module: 8 VRAMs)

Address Bus: Ra[9:0]	(8 x 7 pF + tracking)	max	60 pF
Control: RAS/SC/SE/DSF	(8 x 8 pF + tracking)	max	68 pF
Control: WE/DT	(4 x 8 pF + tracking)	max	36 pF
Control: CAS	(2 x 8 pF + tracking)	max	20 pF
Data Bus: Rd[31:0]	(2 x 9 pF + tracking)	max	25 pF

4.3 Drive Capability

Data Bus I/O: Rd, Vcd, Ud	min	200	pF
QSF	min	50	pF

4.4 Power Consumption Allowance

DRAM Port

It is possible for the architecture to support random reads and writes to non-sequential memory locations with the cache disabled and thereby cause continued access to main memory at full system memory bandwidth; that is, continual N-cycle accesses occurring at 6.4 MHz (ie. 5 cycles of the 32MHz system clock), or 156 ns. CBR Refresh draws a similar amount of current to random read/writes and occurs at a rate of only one 156 ns cycle every 16 uS. It can not therefore affect the maximum overall current consumption by more than 1%.

The DRAM port figures given below for maximum operating current are therefore directly comparable with device datasheet figures which assume the device is performing random read/writes at a minimum address cycle time (tRC) of 150 ns. These figures should be scaled accordingly if devices are specified at a different minimum tRC.

SAM Port

The SAM sends data to VIDC at a rate of 21.33 MHz (64MHz ÷ 3). It does this when necessary to keep the video FIFO buffer full. This results in a bursty transfer. The maximum video bandwidth is 160MB/s with a 2 MB VRAM system, this has a 64 bit (8 byte) wide video data bus, and is equivalent to a 20MHz (160MHz ÷ 8) SAM clock. Therefore the current consumption for VRAM parts is specified for a cycle time of 50 ns (20 MHz). Current consumption specified for parts at a shorter cycle time than this should be scaled accordingly.

Overall Current Consumption

In a 2MB system with two banks of VRAM, although only one DRAM bank is being accessed at any one time, the other bank is still active, as they are both RAS strobed together. Furthermore, in a 2MB system, both banks of SAM will always be writing out to the screen together. Therefore, in a 2MB system, the current consumption will be two times the 1MB figure at all times.

Figures given for a 1 MByte VRAM module at 5V (± 10%) supply

Maximum operating current (DRAM Port active, SAM standby):	700 mA
Maximum operating current (SAM Port active, DRAM standby):	500 mA
Maximum standby current:	200 mA

Thus, a 1MB VRAM module containing 4 off 256k x 8 parts would require each device to draw less than 125 mA when the SAM port is active, and less than 175 mA when the DRAM port is active.

NB. although these figures show the SAM port to consume less power than the DRAM port, this is due to the fact that the SAM is being operated at around half it's maximum frequency whereas the DRAM port is being operated close to it's maximum.