

Acorn OEM Products



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General introduction

The ARM (Acorn RISC Machine) is a general-purpose 32 bit single-chip microprocessor which uses a Reduced Instruction Set Computer architecture to gain high performance. The ARM efficiently executes high level languages and processes interrupts to provide a cost-effective, high performance processing capability. It is particularly well suited for use in

ARM features

The ARM takes full advantage of a number of useful ideas developed in early RISC designs. It supports virtual memory, has a small optimised instruction set hard-wired into a programmable logic array, a heavily pipelined processor, dedicated registers to handle interrupts and a large memory-to-processor bandwidth.

Pipelining is employed so that all parts of the processing and

Features:

- 32-bit architecture
- 32-bit data bus
- 26-bit address bus
- 64 MByte uniform address space
- simple but powerful instruction set
- good high-level language compiler support
- support for virtual memory systems

Fabricated in low-power-consuming CMOS, the ARM offers improved system performance while reducing overall hardware costs. It has an average execution rate of 4 MIPS and uses a two-phase 8 MHz clock.

Another performance advantage is the processor's ability to support memory operation in burst mode or page mode. In burst mode, data can be continuously streamed to and from memory twice as fast as in random access mode, depending on memory/processor interaction. systems that require both real-time response to external interrupt sources and high processing throughput.

Typical applications include communications systems, signal processing, expert systems and such embedded controller systems as laser printer controllers, network controllers and graphics engines.

memory system can be used every cycle when executing consecutive register-to-register instructions. During each processor cycle, one instruction can control the data path while the system decodes a second instruction for the following cycle and fetches a third from memory.

The technology used is $3-\mu m$ double level metal CMOS; the chip size is 50 square millimetres, packaged in an 84-pin leadless carrier.

- fast interrupt response for real-time applications (average interrupt latency less than 2 micro-seconds, worst case less than 6 micro-seconds)
- average execution rate of 4 Million Instructions Per Second (MIPS)
- Iow-power consumption (0.1 watt typical)
- single +5 volt supply

A c o r n R I S C M a c h i n e

• 84-pin JEDEC B leadless chip carrier

A c o r n O E M P r o d u c t s

The instruction set

As a RISC machine, the ARM has an instruction set of only 44 basic instructions. Each instruction has a field containing a condition code that causes an instruction to be skipped if the condition specified by the field is not true. This results in efficient code which executes very quickly. To support the moving of processing functions from hardware to software, the ARM contains 25 32-bit registers, which partially overlap. This overlapping allows fast interrupts to occur without implementing the time-consuming task of storing the contents of the

Performance

The ARM microprocessor has been specifically designed for high performance functions such as real time artificial intelligence and high level language applications. The Acorn chip is smaller and the architecture simpler than conventional microprocessors, yet its execution rate of 4 MIPS is one of the fastest available.

The ARM performance may be summarised as:

ARM evaluation

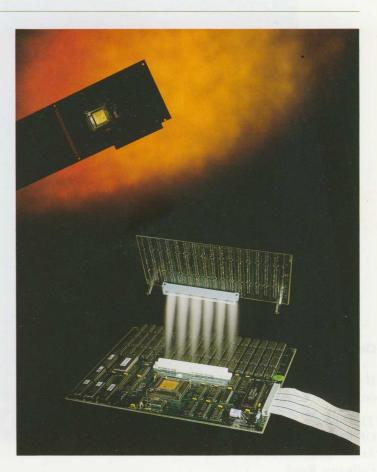
Acorn has two evaluation systems available: one uses the BBC Microcomputer as an I/O device and the other uses the IBM PC (or any PC Compatible) as an I/O device. The former is in the form of a Second Processor for the BBC Micro and the latter is a standard plug-in card for the IBM PC or PC compatible. Both evaluation devices have 4 megabytes of RAM and include five high-level languages, the necessary software tools and a full and comprehensive set of documentation.

The high level languages included are:

LISP Prolog Fortran C BBC Basic register array. The ARM is optimised for low interrupt latency and support of high-level languages.

The instructions are all 32-bits wide (one word) and the instruction set consists of five basic types:

- Branch and branch with link
- Data operation between registers
- Single register data transfer
- Multiple register data transfer
- Supervisor calls
- approximately 4 MIPS average using 150 ns row access DRAMS
- 8 MIPS peak
- Equivalent to:
- 2 to 4 × DEC VAX 11/780 running high level benchmarks
- 10 × IBM PC AT running BASIC benchmarks
- a 16.67 MHz Motorola 68020



Acorn RISC Machine

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Order details

If you wish to order, either write, telex or send your standard order form to:

The Manager OEM Sales Department Acorn Computers Ltd Fulbourn Road Cherry Hinton Cambridge CB1 4JN

Tel. 0223 245200 Telex 817875 ACORN G

and include the following details:

| Product description | Product code |
|--|--------------|
| ARM Evaluation System (for the BBC Micro) | ANC13 |
| PC Evaluation System (for IBM PC or PC compatible) | ANC15 |

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